Amendments to the Specification:

Please replace the paragraph [0086], with the following amended paragraph:

[0086] FIG 13 is a flow diagram illustrating the process 2000 for determining V1(delay) & V2(delay) control voltage functions from the group delay circuit 201. The present invention utilizes two control voltages, referred to as V1 and V2 that are conjunctionally applied (applied at the same time) to respective varactor diodes shown in the previous figures. In addition to the group delay adjuster circuitry it is desirable to provide a process which allows calculation of control voltages V1 and V2. The process is based on maintaining a desired group delay that is provided from an external signal source such as a network ~~analyser~~ analyzer. It is also desirable to use the control voltages to maintain group delay circuit performance.

Please replace the paragraph [0102], with the following amended paragraph:

[0102] Analog outputs 21A and 21B of the dual A/D converter 20 are level shifted and buffered by first driver 22A and second driver 22B ~~respectivly~~ respectively. Drivers 22A and 22B are conventionally constructed by methods known to those skilled in the art. The analog driver outputs 18A and 18B are applied to respective first 16A and second 16B varactors in the group delay adjusting circuit, and were described previously as control lines 212 and 213. Typical circuit implementations may specify that the length of analog lines (212 and 213) be of certain length and to be filtered accordingly.

Please replace the paragraph [0103], with the following amended paragraph:

[0103] Referring to FIG. 14 and FIG. 15 a method for providing digital group delay control 2100, is applied to a group delay adjusting circuit. When group delay adjusting circuit is supplied with power 38 (of FIG. 15) the microprocessor 24 (of FIG. 15) recalls delay functions (V1 and V2) from ~~non-volatile~~ non-volatile random access memory (NVRAM) 34 (of FIG. 15). Upon successful start up the

microprocessor 24 (of FIG. 15) calculates V1 and V2 values for a medium value of delay 2105 (of FIG. 14). The start up delay value can be selected anywhere between minimum and maximum group delay values selected as previously described. The group delay circuit is now placed into active operation, as described in update loop 2110 (of FIG. 14).